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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,038	08/26/2003	Alexander E. Andreev	03-0933/L13.12-0240	2425

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EXAMINER	
CHAUDRY, MUJTABA M	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 11/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,038	ANDREEV ET AL.	
	Examiner	Art Unit	
	Mujtaba K. Chaudry	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Applicants' response was received September 21, 2006.

- Claims 1-9 are pending and stand rejected.
- The drawings submitted September 21, 2006 are accepted.
- The corrections to the specification are accepted.
- Indication of allowable subject matter for claims 2-4 and 6-9 is withdrawn in light of amendments which raise rejections under 35 USC 112.
- Amendments to independent claims raise new rejections under 35 USC 112.
- Previous rejections under 35 USC 112 are withdrawn in light of new ones.

Application pending.

Response to Amendment

Applicants' arguments/amendments with respect to pending claims 1-9 filed September 21, 2006 have been received. All arguments have been fully considered but are not persuasive. The Examiner would like to point out that this action is made final (See MPEP 706.07a).

Applicants contend, "...Gatherer (prior art of record) does not teach...true parallel processing." The Examiner respectfully disagrees. Gatherer teaches (i.e., col. 2, lines 7-25) interleavers to permute data by reading in chunks of data and **writing in parallel** into banks up to an address contention at a bank. The larger the number of banks and corresponding write circuits, the larger the chunk size and the greater the average number of parallel writes.

Applicants contend, "...Gatherer (prior art of record) does not teach...using a routing multiplexer system comprising a plurality of modules..." The Examiner respectfully disagrees. Savage, which was combined with the Gatherer reference teaches (i.e., Figure 7.20 and page 310) routing multiplexers with a plurality of modules.

Applicant contends, "...Gatherer (prior art of record) does not teach...providing permutations." The Examiner respectfully disagrees. Savage teaches (i.e., page 310) a permutation network in the process from the inputs to the outputs.

The Examiner disagrees with the Applicants and maintains rejections with respect to pending claims 1-9. All arguments have been considered. It is the Examiner's conclusion that pending claims 1-9, as presented, are not patentably distinct or non-obvious over the prior art of record.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- Claim recites, "**A parallel turbo decoder routing multiplexer system**..." It is not clear if the claim is directed for a "parallel turbo decoder" or a "routing multiplexer system". It cannot be both.

- Claim recites, "...**p outputs based on a selected permutation of n interleaver memory inputs**..." It is not clear what the Applicants intend to convey. Are there n interleavers which receive and interleave data? Or is there one interleaver with n inputs?
- Claim recites, '...**a first group of p/2 of the modules being coupled to p of the n interleaver memory inputs and a second group of p/2 of the memory modules being coupled to the p outputs**..." Firstly, nowhere does the claim make connection of p outputs with the modules. There are essential structural elements missing from the claim language. Secondly, the limitation "...coupled to p of the n interleaver memory inputs..." is not clear because p is defined to the be the number of outputs and n is the number of inputs wherein n is greater than/equal to p. Examiner has exhaustively attempted to decipher these claim limitations but it is not possible.
- Claim recites, "...**respective ones of the modules**..." which is not accurate. Perhaps stating "...respective one of the plurality of the modules..." would be clear.

Appropriate correction/clarification is requested.

Claim 2 recites the limitation "**multiplexer system**" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim 3 recites the limitation "**multiplexer system**" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim 4 recites the limitation "**multiplexer system**" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- Claim recites, "**...wherein p is an integer variable...**" which does not define p.
- Claim recites, '...**map inputs coupling an output of each memory to respective ones of the first and second inputs of a first group of p/2 of the modules; map outputs coupled to respective ones of the first an second outputs of a second group of p/2 of the modules...**" The claim make no connection between the p memories and the p/2 modules (first and second). There are essential structural elements missing from the claim language.

Appropriate correction/clarification is requested.

Claim 6 recites the limitation "**mapping apparatus**" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim 7 recites the limitation "**mapping apparatus**" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim 8 recites the limitation "**mapping apparatus**" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim 9 recites the limitation "**mapping apparatus**" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gatherer et al. (USON 6603412) further in view of Models of Computation (by John E. Savage pages 309-311, Applicants' IDS).

As per claim 1, Gatherer et al. (herein after: Gatherer) substantially teaches (Figures 1a and 1b) a quasi-parallel read/write interleaver architecture for data blocks by sequential spreading of variable size data subblocks into memory banks with bank address contention initiating the next data subblock. Iterative Turbo decoders with MAP decoders use such quasi-parallel interleavers and deinterleavers. In particular, in a preferred embodiment, Gatherer teaches interleavers to permute data by reading in chunks of data and writing in parallel into

banks up to an address contention at a bank. The larger the number of banks (and corresponding write circuits), the larger the chunk size and the greater the average number of parallel writes.

Gatherer does not explicitly teach a plurality of modules where each has two inputs and two outputs as stated in the present application.

However, Savage teaches, in an analogous art, (page 310, Figure 7.20) a plurality of modules wherein each has two inputs and two outputs. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to use multiple modules with two inputs and two outputs within the teaching of Gatherer. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill would have recognized that by having multiple modules with two inputs and outputs would have increased efficiency as stated by Savage (page 311).

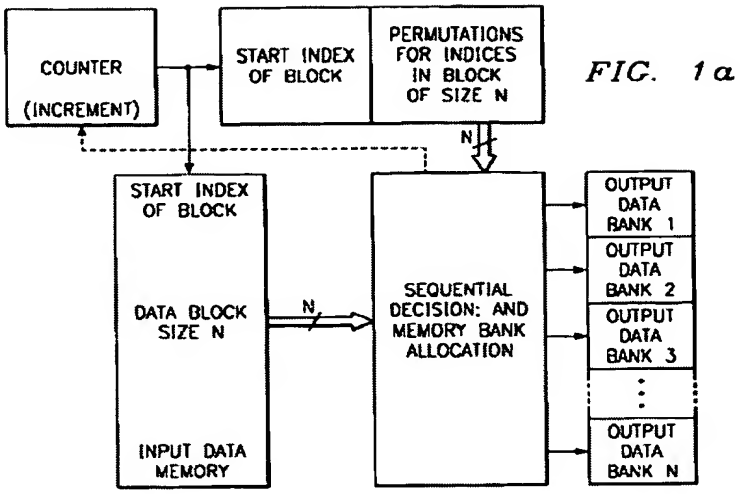

FIG. 1a

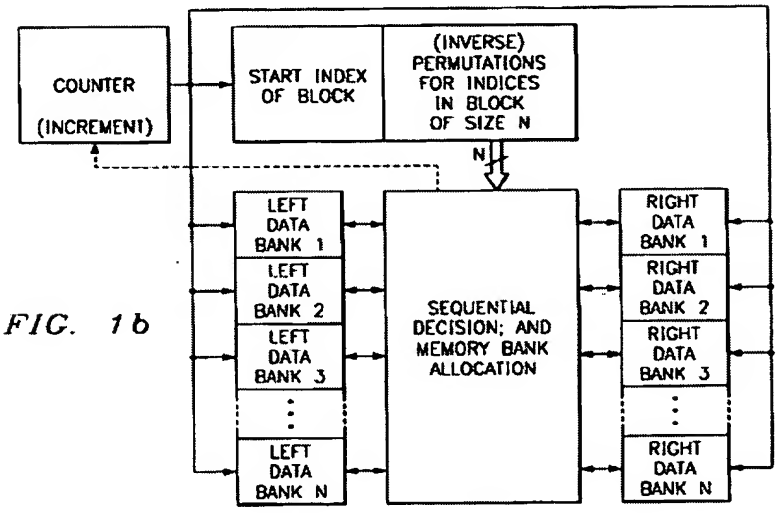

FIG. 1b

As per claim 5, Gatherer teaches (Figures 1a and 1b) a quasi-parallel read/write interleaver architecture for data blocks by sequential spreading of variable size data subblocks into memory banks with bank address contention initiating the next data subblock. Iterative Turbo decoders with MAP decoders use such quasi-parallel interleavers and deinterleavers. In particular, in a preferred embodiment, Gatherer teaches interleavers to permute data by reading in chunks of data and writing in parallel into banks up to an address contention at a bank. The

larger the number of banks (and corresponding write circuits), the larger the chunk size and the greater the average number of parallel writes.

Gatherer does not explicitly teach a plurality of modules where each has two inputs and two outputs as stated in the present application.

However, Savage teaches, in an analogous art, (page 310, Figure 7.20) a plurality of modules wherein each has two inputs and two outputs. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to use multiple modules with two inputs and two outputs within the teaching of Gatherer. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill would have recognized that by having multiple modules with two inputs and outputs would have increased efficiency as stated by Savage (page 311).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 571-272-3817. The examiner may normally be reached Mon – Thur 6:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 571-272-3819.

Mujtaba Chaudry
Art Unit 2133
November 20, 2006

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
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